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National Institute of Technology Hamirpur
Department of Electronics and Communication Engineering Dated: 1-12-2023
B.Tech ECE Dual Degree
End Semester Examination – Nov/Dec 2023

Course :VLSI TEST AND TESTABILITY
Course number : EC-737
Date : 01/12/2023
Duration : 2:30PM- 5:30PM
Semester: VII
Answer all Questions
Maximum marks : 50

1. Find the test vector to determine the **S-A-1** fault at node **h** in Fig.1 using truth table method. (5)

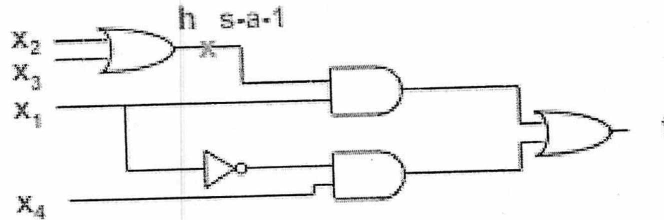

Fig.1

2 a) Find the test set to determine the S-A-0 fault at node B in the Fig.2(a) using Boolean difference method. (5)

b) Find the test set to test S-A-0 fault at node e in Fig.2(b) using Boolean Difference method.

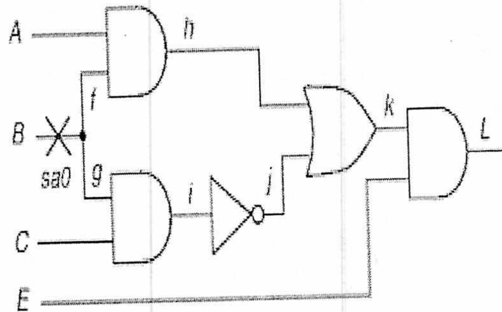

Fig.2(a)

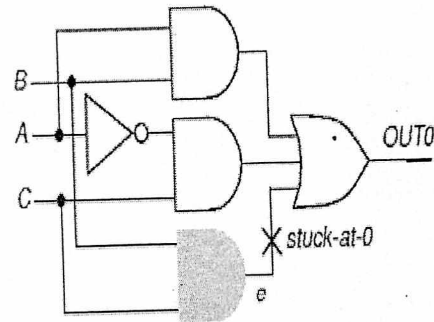

Fig.2(b)

3. Explain the genetic algorithm for simulation based ATPG. (5)

4. a) Explain fault equivalence of 2 input AND and OR gate for stuck at 0 and stuck at 1 fault at the output, respectively. (3)

b) Define terms Controllability and Observability. (2)

5. Explain Logic BIST system and its classification with neat diagram. (5)

[P.T.O]

6. a) Brief about controlling value and inversion value for a combinational circuit and discuss how the gate evaluation is carried out by input scanning. (4)

b) Illustrate the bridging fault model for "X dominates Y if X=1". (1)

7. Demonstrate the application of the D algorithm by deriving a test for detecting the g→s-a-0 fault in the circuit given in Fig. 3. (5)

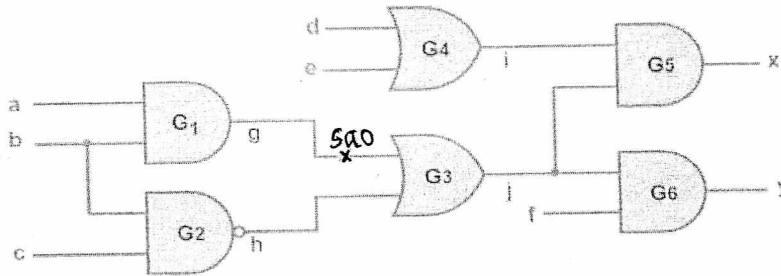

Fig.3 Circuit under test for D Algorithm

8 a) Explain Logic BIST system and its classification with neat diagram. (3)
b) What is meant by hazards? Mention its types and how they are detected. (2)

9. Illustrate the application of PODEM algorithm using the logical circuit shown in Fig.4. Derive test vector for the circuit considering wire g with S-A-0 fault. (5)

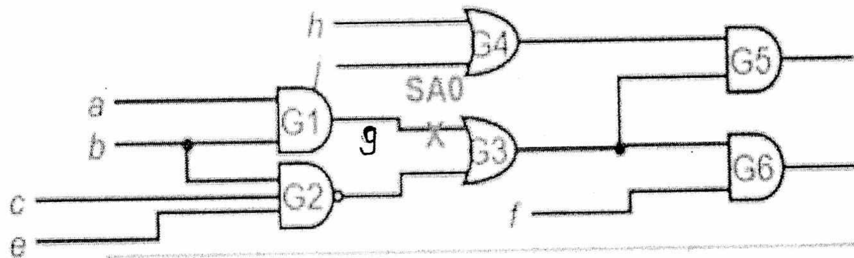

Fig.4 Circuit under test for PODEM Algorithm

10 a) Construct a pseudo random sequence generator using the primitive polynomial $1+x+x^4$ with external XOR LFSR. Identify the proper seed value for the LFSR to get the maximal length sequence. (3)

b) Brief about Shorts and Opens in Wires. (2)