Dr Ankita

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(63)

Electronics and Communication Engineering Department NIT Hamirpur (HP)
End Semester Examination - November 2023

Semester: 7th **ECE**

Sub: Computer Architecture & Organization **Code: EC-455**

Max. Marks = 50 **Time = 3:00 Hrs**

Note:

1. All questions are compulsory
2. Assume suitable data whenever necessary

Q1. a) Multiply 1001 (multiplicand) with 1101 (multiplier), where both binary representations are unsigned, using sequential circuit binary multiplier, give each step of multiplication by giving the contents of Carry register (C), accumulator register (A) and register with Multiplier loaded initially (Q). (3+3)

b) Draw blog-diagram configuration for a sequential circuit binary multiplier using Multiplexer, shift register and control sequencer.

Q2. a) Using Booth algorithm multiply 01011 (multiplicand) with 00111 (multiplier), assuming both binary representations to be signed. (3+3+3)

b) Using Booth algorithm multiply 01011 (multiplicand) with 00111 (multiplier), assuming both binary representations to be signed, but this time use **Booth pair recoding**, i.e., reducing 00111 to three-digit multiplier.

c) Use Carry save addition (CSA) to multiply 101100 (multiplicand) with 111111 (multiplier), assuming both to be unsigned bit representations. Write down every step explicitly along with number of levels used.

Q3. Assume a processor is communicating with the main memory and the aim is to load data into the cache from main memory in case of a **miss**. A cache with **16-word** block is used. It takes 1-clock cycle to send an address to main memory. The first word in the memory is accessed with 8 clock cycles but subsequent words of the block are accessed with 4 clock cycles per word. One clock cycle is needed to send one word to cache. The aim is to load the desired block into the cache. (2+4+2)

a) **If there is no division of memory in modules or just a single memory module is used,** find the time needed to load the desired block into cache.
b) Suppose the last 3 bits of main memory address is used to address the modules and there are **no** nonexistent memory locations. Then, **assuming memory interleaving, find the time needed to load the desired block into cache.**
c) By what factor does the memory interleaving reduces the block transfer time when compared with no memory interleaving for the assumed data.

Q4. Assume for an average program 40% of its instructions are performing read or write operations. Assume also that the memory hierarchy is such that there is a primary cache, a secondary cache and a main memory. The total time needed to load the block from main memory to primary cache is 18 clock cycles (Miss Penalty). Hit rate for primary cache is 95% (3+2+2)

for instructions and 90% for data and the same exist for secondary cache too. Time needed to access primary cache is 1 clock cycle and secondary cache is 10 clock cycles.

a) Find the average access time experienced by the processor.

b) Assume that in absence of caches, a typical DRAM main memory is used that offers 10 clock cycles for every main memory access. Find the improvement in time taken when primary and secondary caches are used along with main memory **over when only the DRAM main memory accesses are there.**

c) Now suppose primary cache is so big that it can accommodate every data that is ever required by the processor, for such a scenario calculate the improvement in performance over having primary and secondary caches along with main memory.

Q5. a) Consider the following analogy for the concept of caching. A serviceman comes to a house to repair the heating system. He carries a toolbox that contains a number of tools that he has used recently in similar jobs. He uses these tools repeatedly, until he reaches a point where other tools are needed. It is likely that he has the required tools in his truck outside the house. But, if the needed tools are not in the truck, he must go to his shop to get them. Suppose we argue that the toolbox, the truck, and the shop correspond to the L1 cache (primary cache), the L2 cache (secondary cache), and the main memory of a computer. How good is this analogy? Write down its correct and incorrect features. (3+3)

b) Suppose a matrix **A** is stored in a row major format in the cache, i.e., first all entries of row-one are stored then entries of row-two and henceforth. You have two pseudocode snippets as given below. Which of these snippets offer better processor performance and why? What principle have you used for determining their performance.

```
int sum_array_1(int a[M][N])
{
int i, j, sum=0;
for (i=0; i<M; i++)
  for (j=0; j<N; j++)
    sum+=a[i][j];
return sum
}
```

```
int sum_array_2(int a[M][N])
{
int i, j, sum=0;
for (j=0; j<N; j++)
   for (i=0; i<M; i++)
      sum+=a[i][j];
return sum
}
```

Q6. a) Use a carry look ahead logic to design a 64-bit adder using 4-bit adders, the configuration of adder should be such that carry look ahead logic is used at every level. Assume a practical fan-in limit of 5 for a logic gate for designing the levels of the adder. Draw the block diagram of the resulting 64-bit adder. (4+3)

b) Calculate the time-delay required for s_{63}, c_{64} and c_{63} using the aforementioned carry lookahead adder and compare it with the time-delay of 64-bit ripple carry adder for s_{63}, c_{64} and c_{63} and write down your observations.

Q7. a) What do you mean by pipelining, explain how does it increase the throughput of the entire workload. (3+4)

b) What are the various hazards associated with pipelining, write a note on each one of them. How those hazards can be resolved.