Do Ashrany Ram

Name: ..... Roll No.: ..... National Institute of Technology, Hamirpur (HP) Name of Examination: B. Tech. (Nov-2023) 5<sup>th</sup> Branch Semester ECE Course Name Course Code : EC-432 • **Electronic Device Modeling Time: 3 Hours** Maximum Marks: 50 Note: 1) Attempt all the questions. 2) Assume suitable data if required. Q1. Drive the equation for recombination rate R, and also explain how it is used in determining of (10) forward & reverse current of a p-n junction structure. Determine the equation of diode current for a p+-n Junction diode. 02. (a) (5) (b) Draw the energy band diagram of a n-MOS structure in accumulation, depletion and inversion (5) mode of operation. Q3. (a) Discuss the impact of substrate bias on threshold voltage of MOSFET. Explain its importance (5) (b) Explain the Sub-threshold Slope for a MOSFET and determine formula for the same. Also (5) derive the equation for minimum sub-threshold slope. With the knowledge that  $\mu_p \approx 0.4 \mu_n$ , what must be relative width of n-channel and p-channel Q4. (a) (5) MOSFET devices if they are to have equal drain currents when operated in saturation mode with overdrive voltage of same magnitude? An n-channel MOSFET device in a Technology for which oxide thickness is 20 µm, (b) (5) minimum gate length 1  $\mu$ m, k<sub>n</sub>= 100  $\mu$ A/V<sup>2</sup> and V<sub>t</sub> = 0.8 V operates in saturation region with small VDS and with gate-source voltage in the range of 0 V to + 5 V. What device width is needed to ensure that minimum available resistance is 1 K $\Omega$ ? Q5. Explain the Eber Moll's level-1, level-2, and level-3 model of BJT. Also mention limitations of (10) each level.